WHAT IS CLAIMED IS:

1. Semiconductor equipment comprising:

a semiconductor substrate with a semiconductor layer embedded therein having a principal side, a rear side opposite to the principal side, and a trench disposed in the rear side of the substrate; and

a vertical type transistor having a first electrode disposed in the principal side of the substrate, a second electrode disposed in the rear side, and a diffusion region disposed in the principal side,

wherein the first electrode connects to the diffusion region through an interlayer insulation film, and

wherein the second electrode is disposed in the trench and connects to the semiconductor layer exposed in the trench.

2. The semiconductor equipment according to claim 1,

wherein the first electrode includes a first metal layer, and the second electrode includes a second metal layer.

3. The semiconductor equipment according to claim 1,

wherein the trench has a taper shape.

4. The semiconductor equipment according to claim 1,

wherein the trench is filled with the second metal layer.

5. The semiconductor equipment according to claim 1,

wherein the vertical type transistor is a metal oxide

semiconductor transistor, and

wherein the first electrode provides a source electrode of the metal oxide semiconductor transistor, and the second electrode provides a drain electrode of the metal oxide semiconductor transistor.

6. The semiconductor equipment according to claim 5,

wherein the semiconductor layer includes a first semiconductor layer having a first conductive type and a second semiconductor layer having the first conductive type, the second semiconductor layer being disposed on the first semiconductor layer and having a low dope concentration lower than that of the first semiconductor layer,

wherein the trench reaches the first semiconductor layer, and

wherein the metal oxide semiconductor transistor includes a drain provided by the first semiconductor layer, a channel diffusion region having a second conductive type and disposed on a surface portion of the second semiconductor layer, the diffusion region as a source diffusion region having the first conductive type and disposed on a surface portion of the channel diffusion region, and a gate electrode contacting a part of the channel diffusion region through a gate insulation film.

7. The semiconductor equipment according to claim 6,

wherein the semiconductor substrate includes a silicon on insulator substrate having an insulation film embedded therein,

wherein the fist and second semiconductor layers are disposed

on the principal side with respect to the insulation film, and

wherein the trench penetrates the insulation film and reaches the first semiconductor layer.

8. The semiconductor equipment according to claim 6,

wherein the metal oxide semiconductor transistor further includes a drain connection diffusion region having the first conductive type, and

wherein the drain connection diffusion region is disposed from a principal side surface of the second semiconductor layer to the first semiconductor layer so as to contact the first semiconductor layer.

9. The semiconductor equipment according to claim 6,

wherein the gate electrode penetrates the channel diffusion region, and reaches the second semiconductor layer.

10. The semiconductor equipment according to claim 1,

wherein the vertical type transistor is an insulated gate bipolar transistor, and

wherein the first electrode provides an emitter electrode of the insulated gate bipolar transistor, and the second electrode provides a collector electrode of the insulated gate bipolar transistor.

11. The semiconductor equipment according to claim 10,

wherein the semiconductor layer includes a third

semiconductor layer having a second conductive type, and a fourth semiconductor layer having the first conductive type and disposed on the third semiconductor layer, and

wherein the insulated gate bipolar transistor includes a collector provided by the third semiconductor layer, a channel diffusion region having the second conductive type and disposed on a surface portion of the fourth semiconductor layer, the diffusion region as an emitter diffusion region having the first conductive type and disposed on a surface portion of the channel diffusion region, and a gate electrode contacting a part of the channel diffusion region through a gate insulation film.

12. The semiconductor equipment according to claim 11,

wherein the semiconductor substrate includes a silicon on insulator substrate having an insulation film embedded therein,

wherein the third and fourth semiconductor layers are disposed on the principal side with respect to the insulation film, and

wherein the trench penetrates the insulation film, and reaches the third semiconductor layer.

13. The semiconductor equipment according to claim 11,

wherein the insulated gate bipolar transistor further includes a collector connection diffusion region having the second conductive type, and

wherein the collector connection diffusion region is disposed from a principal side surface of the second semiconductor layer to the third semiconductor layer so as to contact the third

semiconductor layer.

14. The semiconductor equipment according to claim 11,

wherein the gate electrode penetrates the channel diffusion region, and reaches the fourth semiconductor layer.

15. The semiconductor equipment according to claim 1,

wherein the vertical type transistor is a bipolar transistor, and

wherein the first electrode provides an emitter electrode of the bipolar transistor, and the second electrode provides a collector electrode of the bipolar transistor.

16. The semiconductor equipment according to claim 15,

wherein the semiconductor layer includes a fifth semiconductor layer having the first conductive type and a sixth semiconductor layer having the first conductive type, the sixth semiconductor layer being disposed on the fifth semiconductor layer and having a low dope density lower than that of the fifth semiconductor layer, and

wherein the bipolar transistor includes a collector provided by the fifth semiconductor layer, a base diffusion region having the second conductive type and disposed on a surface portion of the sixth semiconductor layer, the diffusion region as an emitter diffusion region having the first conductive type and disposed on a surface portion of the base diffusion region, a base connection diffusion region having the second conductive type, disposed on a

surface portion of the base diffusion region and having a low dope density lower than that of the base diffusion region, and a base electrode provided by the first electrode.

17. The semiconductor equipment according to claim 16,

wherein the semiconductor substrate includes a silicon on insulator substrate having an insulation film embedded therein,

wherein the fifth and sixth semiconductor layers are disposed on the principal side with respect to the insulation film, and

wherein the trench penetrates the insulation film, and reaches the fifth semiconductor layer.

18. The semiconductor equipment according to claim 16,

wherein the bipolar transistor further includes a collector connection diffusion region having the first conductive type, and

wherein the collector connection diffusion region is disposed from a principal side surface of the sixth semiconductor layer to the fifth semiconductor layer so as to contact the fifth semiconductor layer.

19. The semiconductor equipment according to claim 7,

wherein the semiconductor substrate further includes a separator for surrounding a main part of the vertical type transistor, and

wherein the separator reaches the insulation film so that the main part of the vertical type transistor is isolated from surroundings by the separator.

20. The semiconductor equipment according to claim 7, wherein the trench has a sidewall covered with a sidewall insulation film, and

wherein the second metal layer disposed in the trench is isolated from surroundings by the sidewall insulation film.

21. The semiconductor equipment according to claim 1, wherein the semiconductor equipment is mounted on a printed circuit board by a flip chip mounting method in such a manner that the principal side of the substrate faces the printed circuit board.

22. The semiconductor equipment according to claim 1, wherein the second metal layer is connected to a heat sink with solder.

23. The semiconductor equipment according to claim 1, wherein the semiconductor equipment is mounted in a multi-layer printed circuit board in such a manner that the semiconductor equipment is embedded in the multi-layer printed circuit board.

24. The semiconductor equipment according to claim 1, wherein the vertical type transistor includes a plurality of transistors for providing a multi-channel switch.

25. The semiconductor equipment according to claim 24, wherein the multi-channel switch further includes an electric

load impedance, and

wherein a plurality of transistors and the electric load impedance are disposed between a power source and a ground for providing a high side switch, in which the vertical type transistor is disposed on a power source side and the electric load impedance is disposed on a ground side.

26. The semiconductor equipment according to claim 24,

wherein the multi-channel switch is used for a H-bridge circuit for driving an electric load impedance.

27. Semiconductor equipment comprising:

a semiconductor substrate; and

a metal oxide semiconductor transistor disposed on the semiconductor substrate,

wherein the semiconductor substrate includes a first semiconductor layer and a second semiconductor layer,

wherein the first semiconductor layer has a first conductive type for providing a drain of the metal oxide semiconductor transistor,

wherein the second semiconductor layer has the first conductive type, is disposed on the first semiconductor layer, and has a low dope density lower than that of the first semiconductor layer,

wherein the metal oxide semiconductor transistor includes a channel diffusion region, a source diffusion region, and a gate electrode,

wherein the channel diffusion region has a second conductive type, and is disposed on a surface portion of the second semiconductor layer,

wherein the source diffusion region has the first conductive type, and is disposed on a surface portion of the channel diffusion region,

wherein the gate electrode contacts a part of the channel diffusion region through a gate insulation film, and

wherein the first semiconductor layer includes a trench disposed from a surface of the first semiconductor layer to the second semiconductor layer, and a metal layer as an electrode disposed in the trench.

28. Semiconductor equipment comprising:

a semiconductor substrate provided by a silicon on insulator substrate having an insulation film embedded therein; and

a metal oxide semiconductor transistor disposed on the semiconductor substrate,

wherein the semiconductor substrate includes a first semiconductor layer and a second semiconductor layer, which are disposed on a principal side of the substrate with respect to the insulation film,

wherein the first semiconductor layer has a first conductive type for providing a drain of the metal oxide semiconductor transistor,

wherein the second semiconductor layer has the first conductive type, is disposed on the first semiconductor layer, and

has a low dope density lower than that of the first semiconductor layer,

wherein the metal oxide semiconductor transistor includes a channel diffusion region, a source diffusion region, and a gate electrode,

wherein the channel diffusion region has a second conductive type, and is disposed on a surface portion of the second semiconductor layer,

wherein the source diffusion region has the first conductive type, and is disposed on a surface portion of the channel diffusion region,

wherein the gate electrode contacts a part of the channel diffusion region through a gate insulation film,

wherein the semiconductor substrate further includes a trench and a metal layer,

wherein the trench is disposed on a rear side of the substrate opposite to the principal side, is disposed from a rear surface of the substrate, penetrates the insulation film, and reaches the first semiconductor layer, and

wherein the metal layer as an electrode is disposed in the trench and contacts the first semiconductor layer.